IN THE CLAIMS

Claim 1. (Canceled)

Claim 2. (Canceled)

Claim 3. (Canceled)

Claim 4. (Previously Presented) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a sub power-on reset signal;

a reset terminal for receiving an external power-on reset signal; and

a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one of said sub power-on reset signal and said external power-on reset signal,

wherein said main reset signal generator comprises

a plurality of pulse generators for respectively generating pulses on the basis of a transition edge for a corresponding one of said sub power-on reset signal and said external power-on reset signal, and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

Claim 5. (Canceled)

Claim 6. (Currently Amended) A semiconductor integrated circuit comprising:

a plurality of sub reset signal generators for generating a plurality of sub power-on reset signals at timings different for each other, when detecting that a power supply is switched on;

a reset terminal for receiving an external power-on rest signal; and

a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-reset signals and said external power-on reset signal,

wherein said main rest signal generator comprises

a plurality of pulse generators for respectively generating pulses on the basis of a transition edge for a corresponding one of said sub power-on reset signals and said external power-on reset ~~signal , and~~ signal, and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

Claim 7. (Canceled)

Claim 8. (Canceled)

Claim 9. (Canceled)

Claim 10. (Previously Presented) A semiconductor integrated circuit comprising:

a plurality of sub reset signal generators for generating a plurality of sub power-on reset signals at timings different from each other, when detecting that a power supply is switched on;

a plurality of pulse generators for generating pulses on the basis of the plurality of sub power-on reset signals, respectively, at least one of said pulses being a rectangular pulse; and

a composite circuit for synthesizing the pulses to generate a main power-on reset signal.

Claim 11. (Currently Amended) A method of initializing a semiconductor integrated circuit having a plurality of sub reset signal generators including transistors having threshold values, the method comprising the steps of:

generating a plurality of sub power-on reset signals, each according to respective threshold values of each of the transistors, when detecting that a power supply is switched on;

respectively generating ~~pluses~~ pulses on the basis of a transition edge for a corresponding one of said sub power-on reset signals, at least one of said pulses including a rectangular pulse; and

synthesizing the pulses to generate said main power-on reset signals.

Claim 12. (Canceled)

Claim 13. (Canceled)

Claim 14. (Previously Presented) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a sub power-on reset signal;

a reset terminal for receiving an external power-on reset signal supplied from the exterior of the semiconductor integrated circuit; and

a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one of said sub power-on reset signal and said external power-on reset signal,

wherein said main reset signal generator comprises

a plurality of pulse generators, wherein each pulse generator generates a respective pulse on the basis of a respective transition edge which corresponds to one of said sub power-on reset signal and said external power-on reset signal, and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

Claim 15. (Canceled)

Claim 16. (Previously Presented) A semiconductor integrated circuit comprising:

a plurality of sub reset signal generators for generating a plurality of sub power-on reset signals at timings different from each other, when detecting that a power supply is switched on:

a reset terminal for receiving a external power-on reset signal supplied from the exterior of the semiconductor integrated circuit; and

a main reset signal generator for generating a rectangular pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on resets signals and said external power-on reset signal,

wherein said main reset signal generators comprises

a plurality of pulse generators, wherein each pulse generator generates a respective pulse on the basis of a respective transition edge which corresponds to one of said sub power-on reset signal and said external power-on reset signal, and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

Claim 17. (Canceled)

Claim 18. (Previously Presented) A semiconductor integrated circuit comprising:

a plurality of sub reset signal generators for generating a plurality of sub power-on reset signals at timings different from each other, when detecting that a power supply is switched on; and

a main reset signal generator including a plurality of pulse generators for respectively generating pulses on the basis of a transition edge for a corresponding one of said sub power-on reset signals; and

a composite circuit for synthesizing the pulses to generate a main power-on reset signal, wherein

said main reset signal generator generates said main power-on reset signal having pulses respectively corresponding to each of said sub power-on reset signals, when threshold values of transistors formed in said semiconductor integrated circuit are typical values.

Claim 19. (Canceled)

Claim 20. (Previously Presented) A method of initializing a semiconductor integrated circuit having a plurality of sub reset signal generators including transistors having threshold values, the method comprising the steps of:

generating a plurality of sub power-on reset signals, each according to respective threshold values of each of the transistors, when detecting that a power supply is switched on;

respectively generating pulses on the basis of a transition edge for a corresponding one of said sub power-on reset signals, said pulses not overlapping each other when threshold values of transistors formed in said semiconductor integrated circuit are typical values; and

synthesizing the pulses to generate said main power-on reset signal.

Claim 21. (Canceled)